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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KA LEUNG LING, WILLIAM J. SLIVKOFF,
and NEIL EDWARD BIRNS

Appeal 2009-005577
Application 10/802,199[1]
Technology Center 2100

Before JOHN C. MARTIN, CARLA M. KRIVAK, and
JAMES R. HUGHES, *Administrative Patent Judges*.

HUGHES, *Administrative Patent Judge*.

DECISION ON APPEAL[2]

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[1] Application filed March 16, 2004. The real party in interest is NXP, B.V. (Br. 1.)

[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

Appellants appeal from the Examiner's rejection of claims 21-42 under authority of 35 U.S.C. § 134(a). Claims 1-20 have been canceled. (Br. 2.) The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Appellants' Invention

The invention at issue on appeal relates to a microcontroller and method for operating a microcontroller that includes a processor core; a module for processing messages, e.g., control area network (CAN) messages; a data memory including a first segment further including message buffers, and a second segment further including memory-mapped registers; and a memory interface unit allowing the core and module to concurrently access the memory segments, and which arbitrates access to the memory segments when the core and module concurrently access the same memory segment. (Spec. 1:8-13; Spec. 3:1-31.)[3]

Representative Claim

Independent claim 21 further illustrates the invention. It reads as follows:

> 21. A microcontroller that supports a plurality of message objects, comprising:
>
> a processor core that runs applications;
>
> a module that processes incoming messages;

[3] We refer to Appellants' Specification ("Spec.") and Appeal Brief ("Br.") filed June 16, 2008. We also refer to the Examiner's Answer ("Ans.") mailed September 4, 2008.

> data memory including a first memory segment that provides a plurality of message buffers associated with respective ones of the message objects, and a second memory segment that provides a plurality of memory-mapped registers for each of the message objects, the memory-mapped registers for each message object containing respective command/control fields for configuration and setup of that message object; and,
>
> a memory interface unit that permits the processor core and the module to concurrently access a different respective one of the first and second memory segments, and that arbitrates access to the same one of the first and second memory segments when the processor core and the module request concurrent access to the same one of the first and second memory segments.

References

The Examiner relies on the following reference as evidence of unpatentability:

Baji	US 5,513,374	Apr. 30, 1996
Birns	US 6,493,287	Dec. 10, 2002
Birns	US 6,647,440	Nov. 11, 2003
Birns	US 6,715,001	Mar. 30, 2004 (filed Aug. 1, 2000)
Ling	US 6,732,255	May 4, 2004 (filed Aug. 1, 2000)

Rejections on Appeal

The Examiner rejects claims 21-42 under 35 U.S.C. § 102(b) as being anticipated by Baji.

The Examiner rejects claims 21-42 as being unpatentable on the ground of nonstatutory obviousness-type double patenting over U.S. Patent Nos. 6,493,287; 6,647,440; 6,715,001; and 6,732,255.[4]

ISSUES

Based on our review of the administrative record, Appellants' contentions, and the Examiner's findings and conclusions, the pivotal issues before us are as follows:

1. Does the Examiner err in finding Baji discloses a data memory including first and second memory segments, and a memory interface unit as recited in Appellants' claim 21?

2. Does the Examiner err in finding Baji discloses automatically assembling multi-frame, fragmented messages as recited in Appellants' claim 22?

3. Does the Examiner err in finding Baji discloses arbitrating access according to an alternate winner policy as recited in Appellants' claim 27?

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[4] The Examiner makes this rejection in the Office Action mailed January 15, 2008 ("Last Office Action"), in which the Examiner provides a chart comparing the claims of the various patents to the claims in Appellants' application as well as an explanation for the basis of the rejection. The Examiner, however, fails to formally reiterate this rejection in the Answer, but does respond to Appellants' arguments with respect to the rejection (*see* Ans. 16-17). The Examiner has not withdrawn the rejection. Thus, we view the Examiner's omission as harmless error, and address the merits of the rejection, *infra*.

4. Does the Examiner err in finding the cited patents render Appellants' claims unpatentable on the ground of nonstatutory obviousness-type double patenting?

FINDINGS OF FACT (FF)

Baji Reference

1. Baji describes a digital signal processor (DSP) including a DSP Core (3500), a Direct Memory Access (DMA) Controller (DMAC (3000)) including memory-mapped registers (Fig. 4B (e.g., 3010, 3016, 3018)) and a parallel arbiter (2100), instruction memory (1400), and data memory (1900). (Col. 4, l. 56 to col. 9, l. 50; Figs. 1, 4B.)

2. Baji describes that the storage/memory resources (e.g., data memory and instruction memory), as well as the memory-mapped registers, may be independently and concurrently accessed by the DMAC and DSP Core. (Col. 5, ll. 7-24; col. 5, l. 54 to col. 6, l. 2.)

3. Baji describes the parallel arbiter resolving conflicts that occur when the DMAC and DSP core attempt to simultaneously access the same memory resource – i.e., arbitrating access to the memory resources. (Col. 5, l. 65 to col. 6, l. 33.) The parallel arbiter alternates access to the requested resource between the DMAC and DSP Core. (Col. 7, ll. 1-34; col. 7, l. 64 to col. 8, l. 8.)

ANALYSIS

Appellants provide arguments with respect to the Examiner's § 102 rejection and independent claim 21. Appellants also delineate some arguments with respect to each of their remaining independent claims –

claims 28, 35, 38, 41, and 42. Appellants, however, simply reiterate the arguments made with respect to claim 21 for claim 28 (Br. 13-14), claim 35 (Br. 15), claim 38 (Br. 15-16), claim 41 (Br. 16), and claim 42 (Br. 16-17). Appellants provide separate arguments for dependent claims 22 and 27 (Br. 12-13), but do not separately address any of the other dependent claims – dependent claims 23-26 (Br. 12), 29-34 (Br. 14-15), 36 and 37 (Br. 15), and 39 and 40 (Br. 16). Appellants have elected to argue claims 21-42 together as a group with respect to the Examiner's obviousness-type double patenting rejection. Therefore, we select independent claim 21 and dependent claims 22 and 27 as representative of Appellants' arguments and groupings, and we will address Appellants' arguments with respect thereto. 37 C.F.R. § 41.37(c)(1)(vii). *See In re Nielson*, 816 F.2d 1567, 1572 (Fed. Cir. 1987). We have considered only those arguments that Appellants have actually raised in their Brief. Arguments that Appellants could have made but chose not to make in the Brief have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Appellants have the opportunity on appeal to the Board of Patent Appeals and Interferences (BPAI) to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) (citing *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)). The Examiner sets forth a detailed explanation of a reasoned conclusion of anticipation in the Examiner's Answer with respect to representative claim 21 (Ans. 3-4, 8-13, 16-17), claim 22 (Ans. 6, 14), and 27 (Ans. 7, 14-16). The Examiner also sets forth a detailed explanation of a reasoned conclusion of obviousness-type double patenting. (Last Office Action 2-4; Ans. 16-17.) Therefore, we

look to the Appellants' Brief to show error in the proffered reasoned conclusion. *See Kahn*, 441 F.3d at 985-86.

Issue 1: Arguments Concerning the Examiner's Rejection of Claim 21 under 35 U.S.C. § 102(b)

Appellants contend that Baji does not disclose Appellants' recited data memory or memory interface unit. (Br. 8-12.) Specifically, Appellants argue that Baji does not disclose

> a data memory having a first memory segment that provides a plurality of message buffers associated with . . . message objects, and a second memory segment that provides a plurality of memory-mapped registers for each of the message objects . . . containing respective command/control fields . . . , and a memory interface unit that permits the processor core and the module to concurrently access . . . the first and second memory segments, and that arbitrates access to . . . the first and second memory segments when the processor core and the module request concurrent access to the same . . . memory segment.

(Br. 9.) Appellants also contend that:

> the registers of FIG. 4B . . . are internal registers to DMA Controller (DMAC) 3000 [and that] . . . . it is clear that the parallel arbiter 2100 of Baji absolutely does not permit DSP core 3500 and DMAC 3000 to concurrently access . . . the first and second memory segments . . . as cited by the Examiner. It is also clear that parallel arbiter 2100 of Baji absolutely does not arbitrate access to . . . the first and second memory segments . . . when the DSP core 3500 and DMAC 3000 request concurrent access to the same . . . memory segments. Indeed, it does not appear that DSP core 3500 ever requests any access to the second memory segments . . . as alleged by the Examiner. [And, t]herefore, Bali cannot possibly disclose the microcontroller of claim 21!

(Br. 10-11.) Appellants further contend that Baji does not disclose that its data memory and instruction memory (the Examiner's purported first

memory segment) include "a plurality of message buffers associated with each of a plurality of message objects," nor that its memory-mapped registers (the Examiner's purported second memory segment) "contain respective *command/control fields for configuration and setup of that message object*." (Br. 11.)

The Examiner finds that Baji discloses each feature of Appellants' claim 21, and provides a detailed explanation as to why Appellants' arguments fail to overcome the Examiner's anticipation rejection. (Ans. 3-4, 8-13.) Specifically, the Examiner finds that Baji discloses the disputed features of a processor core (DSP Core), a module that processes incoming messages (DMAC, which processes instructions), data memory that includes a first memory segment including a plurality of message buffers associated with message objects (data memory and instruction memory), a second memory segment that includes a plurality of memory-mapped registers for each of the message objects (memory-mapped registers seen in figure 4B), and a memory interface unit (the Parallel Arbiter) that permits the processor core and the module to concurrently access the first and second memory segments, and that arbitrates access to the same memory segments. (Ans. 3-4.) The Examiner also finds that Baji discloses instruction requests that are equivalent to Appellants' recited message objects. (Ans. 3, 4, 12-13.)

Based on the record before us, we do not find error in the Examiner's anticipation rejection of representative claim 21. We agree with the Examiner that Baji discloses the disputed features. We begin our analysis by construing Appellants' disputed claim limitations.

We give claim terminology the "broadest reasonable interpretation consistent with the [S]pecification" in accordance with our mandate that

"claim language should be read in light of the [S]pecification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (citations omitted). We note that the recitation of "message buffers," "message objects," and "command/control fields" (or memory partitions and/or contents generally) constitute non-functional descriptive material. Appellants' recited message buffers, message objects, and command/control fields correspond to memory portions (sections, divisions, pieces, or segments) and data stored in memory. These recitations merely recite what the information or data represents. How a portion of the memory and the data in a memory may be named or labelled (e.g., a "message buffer," a "message object," or a "command/control field") does not functionally change the memory. The acts of storing, identifying, and retrieving data in a memory are the same regardless of how the memory may be subdivided or the data in the memory may be named. Merely labelling a portion of a memory as a buffer, and data as an object (message object), as opposed to some other unique identifier, does not further limit the claimed invention either functionally or structurally. The partitioning of memory and the informational content of the data thus represent non-functional descriptive material entitled to no weight in the patentability analysis. *See Ex parte Curry*, 84 USPQ2d 1272, 1274 (BPAI 2005) (informative), *aff'd*, No. 06-1003 (Fed. Cir. June 12, 2006) (Rule 36) ("wellness-related" data in databases and communicated on distributed network did not functionally change either the data storage system or the communication system used in the claimed method). *See also In re Ngai*, 367 F.3d 1336, 1339 (Fed. Cir. 2004); *Ex parte Nehls*, 88

USPQ2d 1883, 1887-90 (BPAI 2008) (precedential) (discussing non-functional descriptive material).

Accordingly, we broadly but reasonably construe the disputed limitations to mean: 1) a memory including a first segment and a second segment that further includes memory-mapped registers; and 2) a memory interface unit that allows a processor core and a module to concurrently access the first and second segments, and which arbitrates access to the segments when the processor core and the module simultaneously request access to the same segment. This construction is consistent with the cited reference, Appellants' Specification, and the knowledge of those skilled in the art at the time of Appellants' invention.

As detailed in the Findings of Fact section *supra*, Baji describes a DSP Core and a DMAC that processes instructions, instruction memory, and data memory. The DMAC also includes memory-mapped registers, and a parallel arbiter. Baji maps the instruction memory, data memory, and memory-mapped registers so that each memory resource has a predefined unique address – i.e., each memory resources is "memory-mapped." The parallel arbiter allows the DMAC and DSP Core to concurrently and independently access each of the storage/memory resources including the data memory, instruction memory, and memory-mapped registers. The parallel arbiter also arbitrates access to the same memory resource by the DMAC and DSP core when the DMAC and core attempt to simultaneously access the same memory resource. (FF 1-3.) We agree with the Examiner that instructions may be broadly but reasonably construed to be messages.

We therefore find that Baji discloses a DSP Core (the recited processor core), a DMAC that processes instructions (the recited module that

process messages), data memory and instruction memory (the recited first memory segment),memory-mapped registers (the recited second memory segment including memory-mapped registers), and a parallel arbiter (the recited memory interface unit) that allows the DSP Core and DMAC to concurrently access the various memory resources (e.g., the first and second memory segments), and which arbitrates access to the resources. Thus, a broad but reasonable interpretation of Appellants' claim 21 reads on at least one embodiment of Baji.

Moreover, even if we confer, *arguendo*, some weight to Appellants' recited message buffers, message objects, and command/control fields, we find Baji discloses memory containing message (instruction) buffers, message objects, and registers including control fields. Appellants' Specification describes a message buffer as a "block of locations . . . where . . . messages are stored." (Spec. 7, ll. 19-21.) Appellants' Specification also describes a message object as a buffer (e.g., "Receive RAM buffer" or "Transmit RAM buffer") or a "communication channel." (Spec. 5:31-36.) Baji discloses memory blocks (e.g., instruction memory) that may store instructions, as well as memory blocks (e.g., data memory) that may store data (i.e., message data) or communication channels (e.g., Busses – *see* Fig. 1; col. 5, ll. 7-24). Baji also discloses memory-mapped registers that have control fields (e.g., Control Register (3018) – *see* Fig. 4B; col. 10, ll. 17-24). In view of Appellants' broad disclosure of message buffers and message objects, we find Baji discloses memory segments including message (instruction) buffers associated with message objects, and memory-mapped registers associated with message objects.

We find Appellants' contrary arguments unpersuasive. Specifically, Appellants mischaracterize Baji, stating that Baji does not allow concurrent access to the DMAC internal registers (*see* Baji, Fig. 4B), nor arbitrate access thereto. (Br. 10-11; *supra*.) Appellants' statements directly contradict the express disclosure of Baji:

> Both the DMAC 3000 and the DSP Core 3500 can independently access almost all memory mapped locations in the external memory 2500, instruction memory 1400, peripheral devices 2300 or data memory 1900 as well as most of the internal registers. By memory mapping all DSP resources, the DSP 1100 also makes all memory mapped resources accessible to the host processor 1200.
>
> Additionally, as discussed above, each of these storage devices, all of which have a single port, can be accessed concurrently by the DMAC 3000 (over DA bus 1112) and the DSP Core 3500 (over at least one of the XA 1108, YA 1110 or PC 1116).

(Baji, col. 5, l. 58 to col. 6, l. 2; *see* FF 2-3.) We find (*supra*) that Baji discloses these features. Further, Appellants' arguments are not commensurate with the scope of the recited claim limitations. Appellants argue that Baji fails to disclose that "DSP core 3500 ever requests any access to the second memory segments." (Br. 11; *supra*.) As pointed out by the Examiner (Ans. 11-12), Appellants' claim does not explicitly (positively) recite that the processor request access to either memory segment, it instead recites that the "memory interface unit . . . permits the processor core and the module to concurrently access . . . the first and second memory segments" – which we construe to mean that the memory interface unit allows or provides the capability for the processor core and the module to concurrently access the first and second memory segments.

In summary, Appellants do not provide any persuasive evidence or argument that Baji fails to disclose the disputed features. Further, Appellants failed to file a Reply Brief to rebut the findings and responsive arguments made by the Examiner in the Answer. Thus, we find Baji discloses Appellants' disputed claim limitations as recited in Appellants' independent claim 21. Appellants do not separately argue independent claims 28, 35, 38, 41, and 42 (*supra*). We, therefore, find Baji anticipates Appellants' claims 21, 28, 35, 38, 41, and 42 for the reasons set forth with respect to representative claim 21. It follows that Appellants do not persuade us of error in the Examiner's anticipation rejection of claims 21, 28, 35, 38, 41, and 42, and we affirm the Examiner's rejection of these claims.

Issue 2: Arguments Concerning the Examiner's Rejection of Claim 22 under 35 U.S.C. § 102(b)

Appellants contend that Baji does not disclose "messages include multi-frame, fragmented messages, and the module automatically assembles the multi-frame, fragmented messages." (Br. 12.) The Examiner finds that Baji discloses "multi-frame, fragmented instructions as seen in tables 1 and 2 in columns 10 – 12," and that the "DMAC 3000 . . . handles the instructions." (Ans. 14; *see* Ans. 6, 14.) Based on the record before us, we do not find error in the Examiner's anticipation rejection of representative claim 22. We agree with the Examiner that Baji discloses the disputed features.

As explained by the Examiner (Ans. 14), Baji describes multi-part (i.e., multi-frame and/or fragmented) instruction handling by the DMAC. For example, each DMAC data transfer operation requires a read operation

and a write operation – i.e., multi-part instruction handling by the DMAC or automatic assembly of the multi-frame, fragmented messages by the module as recited in Appellants' claim.

Further, we note that Appellants attempt to claim the form of the data sent to their recited module, as well as a method of using the recited module. Appellants' claim 22 recites a microcontroller – i.e., an apparatus – not a process. At most, the phrase "the module automatically assembles the multi-frame, fragmented messages" recites an intended use or function of the module. A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham*, 2 USPQ2d 1647, 1648 (BPAI 1987). Similarly, while features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Schreiber*, 128 F.3d 1473, 1477-78 (Fed. Cir. 1997). "[A]pparatus claims cover what a device *is*, not what a device *does*." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1468 (Fed. Cir. 1990). Put simply, how an apparatus invention is used is not germane to whether it is anticipated by the prior art.

Thus, we find Baji discloses Appellants' disputed claim limitation as recited in Appellants' dependent claim 22. We, therefore, find Baji anticipates Appellants' claim 22. It follows that Appellants do not persuade us of error in the Examiner's anticipation rejection of claims 22, and we affirm the Examiner's rejection of this claim.

Issue 3: Arguments Concerning the Examiner's Rejection of Claim 27 under 35 U.S.C. § 102(b)

Appellants contend that Baji does not disclose that "the memory interface unit arbitrates access to the first and second memory segments between the processor core and the module according to an alternate winner policy." (Br. 13.) The Examiner finds that Baji discloses an alternating arbitration scheme. (Ans. 7, 15-16.) Based on the record before us, we do not find error in the Examiner's anticipation rejection of representative claim 27. We agree with the Examiner that Baji discloses the disputed features.

As explained by the Examiner (Ans. 6, 15, 16), Baji describes the parallel arbiter arbitrating access in an alternating manner between the DSP Core and DMAC. (FF 3.) We also note that, as with claim 22 (*supra*), Appellants attempt to claim a method of using the recited memory interface unit. At most, "the memory interface unit arbitrates access to the first and second memory segments between the processor core and the module according to an alternate winner policy, wherein a previous loser is designated a current winner" recites an intended use or function of the unit. As we explain *supra*, such a statement of the manner of intended use of the apparatus does not differentiate the claimed apparatus from a prior art apparatus. *See Schreiber*, 128 F.3d at 1477-78; *Masham*, 2 USPQ2d at 1648. Thus, we find Baji discloses Appellants' disputed claim limitation as recited in Appellants' dependent claim 27.

Appellants do not separately argue dependent claims 23-26, 29-34, 36, 37, 39, and 40 (*supra*). We, therefore, find Baji anticipates Appellants' claims 22-27, 29-34, 36, 37, 39, and 40 for the reasons set forth with respect to representative claims 22 and 27 (*supra*). It follows that Appellants do not persuade us of error in the Examiner's anticipation rejection of claims 22-27,

29-34, 36, 37, 39, and 40, and we affirm the Examiner's rejection of these claims.

Issue 4: Arguments Concerning the Examiner's Obviousness-Type Double Patenting Rejection of Claims 21-42

Appellants contend that the Examiner does not provide a properly detailed analysis with respect to the obviousness-type double patenting rejection, but do not address the substance of the Examiner's rejection. (Br. 17.) The Examiner finds that:

> US Patent Number 6,732,255 recites all of the claim limitations verbatim with the exclusion of a single word CAN which in turn broadens the claimed environment and is deemed obvious. Furthermore the Examiner pointed out the claims were substantially the same as the US Patents 6715001, 6493287 and 6647440 with the exception that the instant application doesn't have the CAN microcontroller environment therefore broadening would dictate obviousness.

(Ans. 17; *see* Ans. 16-17; Last Office Action 2-4.) Based on the record before us, we do not find error in the Examiner's obviousness-type double patenting rejection of claims 21-42. We agree with the Examiner that Appellants' previously issued patents render the claims of the present invention obvious.

A "CAN microcontroller" is merely a specific type of microcontroller. Thus, as explained by the Examiner, Appellants' "CAN microcontroller" claims in U.S. Patent No. 6,732,255 ("255 patent") render the "microcontroller" claims, recited in the present application, obvious because the claims are identical except for the omission of the term "CAN" in the claims of the present application. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007) ("[W]hen a[n] [application] claims a structure already

known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result." (citing *United States v. Adams*, 383 U.S. 39, 50-51 (1966))). It is well established that a claim to a species – a claim narrower in scope – anticipates a generic claim encompassing the species – a claim broader in scope. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 782 (Fed. Cir. 1985) ("It is also an elementary principle of patent law that when, as by a recitation of ranges or otherwise, a claim covers several compositions, the claim is 'anticipated' if one of them is in the prior art.") Also, "'anticipation is the epitome of obviousness.'" *In re Emert*, 124 F.3d 1458, 1462 (Fed. Cir. 1997) (quoting *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 716 (Fed. Cir. 1984)). Thus, we find no error in the Examiner's explanation that "broadening would dictate obviousness." (Last Office Action 3.)

Here, allowing Appellants' broader "microcontroller" claims, would effectively extend the term of their narrower "CAN microcontroller" claims – the exact result that the doctrine of obviousness-type double patenting seeks to prevent:

> a patentee could gain an extension of the term on a species when the broad genus later issued. This practice would extend the exclusionary right past the 17-year limit mandated by Congress. Under Supreme Court precedent, only one patent can issue for each patentable invention. A second application – "containing a broader claim, more generical in its character than the specific claim in the prior patent" – typically cannot support an independent valid patent.

In re Goodman, 11 F.3d 1046, 1053 (Fed. Cir. 1993) (internal citations omitted) (quoting *Miller v. Eagle Mfg. Co.*, 151 U.S. 186, 198 (1894)).

Appellants do not provide any substantive arguments with respect to the Examiner's obviousness-type double patenting rejection. Further, Appellants failed to file a Reply Brief to rebut the findings and responsive arguments made by the Examiner in the Answer. Also, Appellants do not separately argue claims 21-42 with respect to the instant rejection (*supra*). Thus, we find Appellants' previously issued patents render the claims of the present invention obvious. It follows that Appellants do not persuade us of error in the Examiner's obviousness-type double patenting rejection of claims 21-42, and we affirm the Examiner's rejection of these claims.

CONCLUSIONS

Appellants have not shown that the Examiner erred in rejecting claims 21-42 under 35 U.S.C. § 102(b).

Appellants have not shown that the Examiner erred in rejecting claims 21-42 on the ground of nonstatutory obviousness-type double patenting.

DECISION

We affirm the Examiner's rejection of claims 21-42 under 35 U.S.C. § 102(b).

We affirm the Examiner's nonstatutory obviousness-type double patenting rejection of claims 21-42.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(v).

AFFIRMED

msc

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